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JONATHAN Y. KANG, ESQ.
LEE & HONG P.C.
14th Floor
801 S. Figueroa Street
Los Angeles, CA 90017

EXAMINER	
TRUONG, LECHI	
ART UNIT	**PAPER NUMBER**
2194	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,405	SEW, YOU-SUK	
	Examiner	Art Unit	
	LeChi Truong	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are presented for the examination.

Claim Object

2. As to claim 9, it is uncertain what "MAP" means< ie, applicant is required to expand this abbreviation>.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack proper antecedent basis:

The index– claim 10;

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al (US. Patent 6,253293 B1) in view of Ichige et al (US. Patent 5,255,238).

As to claim 1, Rao teaches the invention substantially including included: An interrupt-free interface (critical piece of code must not be interrupt, col 16, ln 14-19/ col 11, ln 36-41), a modem processor (PC users increasingly expect not only audio functionality but high quality sound capability, col 1, ln 60-65/ a first processor, col 2, ln 36-40/ first DSP core 200a, col 5, ln 7-10-15/ col 6, ln 30-34/ col 7, ln 61-67/ col 10, ln 1-5), a multimedia application processor (MAP) (a multimedia application such as gaming and telecommunications. Audio functionality is therefore typical available on most conventional PCs, col 1, ln 55-60/ the second processor, col 2, ln 40-44), a wired or wireless channel (multiple channel, col 3, ln 26-30/ virtual channel, col 10, ln 45-50), a modem processor for processing data received through a wired or a wireless channel from outer side (col 10, ln 45-50/ ln 6-9/ col 3, ln 26-30), performing various controls according to the data receipt(col 7, ln 62-67/ col 10, ln 1-5/ ln 45-50), a multimedia application processor (MAP) for processing information(col 8, ln 1-4, col 10, ln 6-10), voice/sound/moving picture which will be provided to a user(col 1, ln 62-67); a dual access memory(shared memory , col 2, ln 35-40/col 10, ln 12-15/ ln 43-47), an indicator(A/B _message_semaphores/ AB_shared_ memory_semaphores, col 10, ln 12-15 and ln 25-29/ ln 50-55/ col 11, ln 1-6/ ln 8-10), a dual access memory storing an indicator(shared memory of 544 words as well as

communication mailbox consisting registers AB_message_memory_semaphores, col 10, ln 12-35/ semaphore variable which reside in AB_shared _memory, col 10, ln 50-52), storing a dual access memory for storing an indicator for identifying normal transmitting/receiving status of the data (col 11, ln 6/ col 13, ln 45-49/ col 17, ln 9-11/ setting s bit a shared register with the second processor after completing of said step of reading, col 18,l n 37-39).

Rao does not explicitly teach a memory for storing an index for identifying the number of data in case that the data is written or read with a predetermined period. However, Ichige et al teaches a memory for storing an index for identifying the number of data in case that the data is written or read with a predetermined period (FIFO memory 6 includes a bit cell array 12/ A unit storage area of BC array 13 into which data is being written is designated by a write counter 20/ a unit storage area the unit storage area is designed by a read counter 22, col 8, ln 1-5/ ln 19-25/ Fig. 1A, receiving FIFO Memory 6 . . . write counter 20/ the write counter 20 is synchronism with the assert timing of the strobe signal RWS and selects the unit storage are into which the receiving data items are written. The writer counter 20 is subsequently incremented in synchronism with the negate timing of the strobe signal RWS (predetermined period), col 8, ln 31/ ln 40-46/ the receiving FIFO memory 6 on the basic of the count operating of the write counter 20 and the read counter 22. The read counter 22 and the write counter 20 repeat increment in accordance with the read and writer operations. Increment starts from reset states in which count values RCOUNTw are zero, respectively. After each of the counters 22 and 20 has counted to (n-1)(index), col 11, ln 38-36/ When the number of data items stored in the receiving FIFO 6 reaches a pretermined number (predetermined period), the receiving FIFO memory 6

assert a transfer ready, col 7, ln 30-36/ the number of stored data items is calculated on basis of the values of the value of the write counter, col 3, ln 46-51).

It would have been obvious to one of the ordinary skill in the art at the time the invention was to modify the teaching of Rao and Ichige because Ichige a memory for storing an index for identifying the number of data in case that the data is written or read with a predetermined period would improve the efficiency of Rao's system by allowing the frequency of data transfer requests is lowered and the over head time for starting a data transfer control is decreased, whereby throughput of the system can be enhanced.

As to claim 2, Rao teaches wherein the indicator is stored in the dual access memory in order to identify whether the data is normally written or read or not, in case that the data is written or read between the modem processor and the MAP (col 11, ln 6/ col 13, ln 45-49/ col 17, ln 9-11).

As to claim 3, Ichige teaches wherein the index represents the number of data which is written or read and is stored in the dual access memory in case that the data is written or read between the modem processor and the MAP (col 8, ln 31/ ln 40-46 col 11, ln 38-36/ col 7, ln 30-36/ /, col 3, ln 46-51).

As to claim 4, it is an apparatus claim of claims 3 and 4; therefore, they are rejected for the same reasons as claim 3 and 4 above.

5. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al (US. Patent 6,253293 B1) in view of Ichige et al (US. Patent 5,255,238), as applied to claim 1 above, and further in view of Yamauchi et al (US. Patent 5,649102)

As to claim 5, Rao teaches a data storing area for storing data transmitted/received between the modem processor and the MAP (col 2, ln 35-40/ col 10, ln 37-42/ col 16, ln 30-34).

Rao and IChige do not explicitly teach an indicator storing area for storing the indicator representing storing unit/reading unit of the data; and an index storing area for storing the index representing the writing status/reading status of the data. However, Yamauchi teaches an indicator storing area for storing the indicator representing storing unit/reading unit of the data (the shared data management table 405 also has scattering flag entries indicating whether or not shared data to be used by an application is being stored, col 10, ln 36-38/ Fig. 6), an index storing area for storing the index representing the writing status/reading status of the data (shared data scattering number entries 608 indicating the number of scattered shared data sets, col 10, ln 39-40/ Fig. 6).

It would have been obvious to one of the ordinary skill in the art at the time the invention was to modify the teaching of Rao, Ichige and Yamauchi because Yamauchi an indicator storing area for storing the indicator representing storing unit/reading unit of the data; and an index storing area for storing the index representing the writing status/reading status of the data would improve the efficiency of Rao and Yamauchi's systems by allowing the computers related to access to shared data to reduce the wasteful waiting time and to improve the access performance of executing a program.

As to claim 6, Ichige teaches the data storing area comprises two areas for storing the data (col 9, ln 32-34/ col 12, ln 9-12).

As to claim 7, Yamauchi teaches the indicator storing area comprises four areas for storing the data (col 10, ln 36-38/ Fig. 6).

As to claim 8, Yamauchi teaches the index storing area comprises four storing areas for storing the data (col 10, ln 39-40/ Fig. 6)

6. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al (US. Patent 6,253293 B1) in view of Huang et al (US. Patent 6,122,713) and further in view of Engel et al (US. Patent 5,544,329).

As to claim 9, Rao teaches An interrupt-free interface (critical piece of code must not be interrupt, col 16,ln 14-19/ col 11, ln 36-41), a modem processor (PC users increasingly expect not only audio functionality but high quality sound capability, col 1, ln 60-65/ a first processor, col 2, ln 36-40/ first DSP core 200a, col 5, ln 7-10-15/ col 6, ln 30-34/ col 7, ln 61-67/ col 10, ln 1-5), a multimedia application processor (MAP) (a multimedia application such as gaming and telecommunications. Audio functionality is therefore typical available on most conventional PCs, col 1, ln 55-60/ the second processor, col 2, ln 40-44/ the second DSP 200b, col 5, ln 7-10-15/ col 6, ln 30-34/ col 7, ln 61-67/ col 10, ln 1-5), a first step of writing or reading data on a dual access memory from a modem processor or from a MAP (col 16, ln 30-34), second step of deciding whether the data is normally written or read on the dual access memory (col 11, ln 3-5/ col 17,l n 8-14),

Rao does not teach reading or writing after initializing the dual access memory, a third step of examining the storing area of the dual access memory in case that a predetermined time

which is set in advance passed over, a fourth step of reading the data stored in the dual access memory whenever an indicator is changed as a result of the examination, a fifth step of deciding whether the data is normally read or not. However, Haung teaches reading or writing after initializing the dual access memory, a predetermined position of the dual access memory (determines if the local processor has written the shared memory, col 3, ln 9-10), a third step of examining the storing area of the dual access memory in case that a predetermined time which is set in advance passed over (the host examines the high byte of the high to low semaphore to determine if the shared memory 204 is available. If the shared memory is not available in step 412 then the host preferably waits until the shared memory 204 becomes available [a pretermined time which is set in advance passed over], col 8, ln 2025), a fourth step of reading the data stored in the dual access memory whenever an indicator is changed as a result of the examination (If the shared memory 204 is determined to be available in step 414, the step 416 the host sets the low byte of the high to low semaphore to 1 [an indicator is changed as a result of the examination] to inform the broad the host is reading the shared memory, col 8, ln 31-35).; and a fifth step of deciding whether the data is normally read or not(if the board has not written data into the shared memory 204 while the host was reading data from the shared memory 204, then in step 424 the host clears the low byte of the high to low semaphore to indicate completion of the read, col 8, ln 45-48).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Rao and Huang because Huang reading or writing after initializing the dual access memory, examining the storing area of the dual access memory, reading the data stored in the dual access memory, deciding whether the data is normally read or

not would improve the efficiency of Rao system by allowing improved system for enabling dual post access to a shared memory system with high priority and low priority requesters.

Rao and Huang do not teach the predetermine position of memory. However, Engel teaches a predetermine position of memory (a target address has been determined in the subsystem memory for a message, col 15, ln 44-46/ the target address in the subsystem memory are determined by the subsystem interface unit and RAM MAP, the user may transmit messages to the interface station in any order, spread the message apart over time to allow for the largest message size, overlay message areas, or send all illegal message to the same are in the subsystem memory, col 15, ln 4-10).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Rao, Huang and Engel because Engel's a predetermine position of memory would improve the efficiency of Rao and Hang's systems by allowing the subsystem memory to receive the messages without the need for a double buffer or to use any type of interrupt handler.

As to claim 11, Rao teaches wherein the indicator is stored in the dual access memory in order to identify whether the data is normally written or read or not, in case that the data is written or read between the modem processor and the MAP (col 11, ln 6/ col 13, ln 45-49/ col 17, ln 9-11).

7. Claims **10, 12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao et al (US. Patent 6,253293 B1) in view of Huang et al (US. Patent 6,122,713) in view of Engel et al

(US. Patent 5,544,329), as applied to claim 9 above, and further in view of Ichige et al (US. Patent 5,255,238).

As to claim 10, Rao teaches the second step decides whether the data of a unit is normally stored on a predetermined position of the dual access memory or not by setting or resetting the indicator, which represents the normal transmitting/receiving status of the data (col 11, ln 3-5/ col 17, l n 8-14).

Rao, Huang and Engel do not teach increasing the index, which represents the number of data by 1. However, Ichige teaches increasing the index, which represents the number of data by 1(the read counter 22 and the writer counter 20 repeat incrementation in accordance with the read and writer operations, col 11, ln 40-46).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Rao, Huang, Engel and Ichige because Ichige increasing the index which represents the number of data by would improve the efficiency of Rao and Huang systems by allowing the frequency of data transfer requests is lowered and the over head time for starting a data transfer control is decreased, whereby throughput of the system can be enhanced.

As to claim 12, Rao teaches deciding whether the data is normally written or read or not by identifying the indicator representing the normal transmitting/receiving status of the data (col 10, ln 12-35). And Ichige teaches the index representing the number of data with a predetermined period (col 7, ln 30-36 /col 3, ln 46-51).

As to claim 13, Huang teaches decides whether the data is normally read or not by setting or resetting the indicator representing the normal transmitting/receiving status of the data (col 8, ln 45-48). .

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272 3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomson, William can be reached on (571) 272 3718. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

January 8, 2007

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER